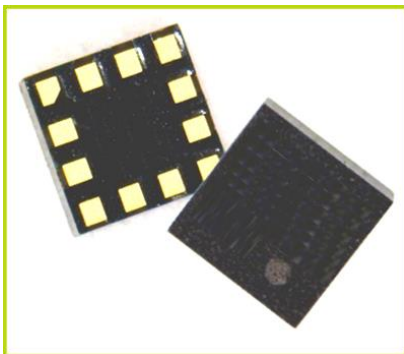


GENERAL DESCRIPTION

The MC3451 is a low-noise, integrated digital output 3-axis accelerometer with a feature set optimized for smartphones and smart watches. Applications include user interface control, gaming motion input, tilt function, gesture recognition, pedometer, display orientation, and power saving for handheld and wearable devices.

The MC3451 internal sample rate can be set from 0.25 to 256 samples / second. The integrated smart processing unit performs pedometer and gesture functions without any external components. The device also contains a 2K byte flexible first-in, first-out (FIFO) buffer to store data for access via the internal Smart Logic Unit or via the I2C interface to an external host processor.

The MC3451 is available in a 12-pin LGA package and is guaranteed to operate over an extended temperature range from -40°C to +85°C.



FEATURES

Range, Sampling & Power

- ± 2 , 4, 8, 12 or 16g ranges
- 8, 10 or 14-bit resolution
- Sample rate of 0.25 - 256 samples/sec
- Low standby current of 4 μ A
- 300 μ A gesture mode typical current
- Integrated high-performance pedometer
- Integrated gesture processing unit

Event Detection

- Independent X,Y,Z Tap
- Any motion
- Gesture detect
- Low-noise architecture minimizes false triggering

Simple System Integration

- I2C interface, up to 400 kHz
- 2K byte flexible FIFO
- 2 x 2 x 0.93 mm 12-pin LGA package
- Single-chip 3D silicon MEMS
- 125 μ g/ $\sqrt{\text{Hz}}$ noise
- RoHS and “Green” compliant

TABLE OF CONTENTS

- 1 Order Information..... 4
- 2 Functional Block Diagram 5
- 3 Packaging and Pin Description 6
 - 3.1 Package Outline..... 6
 - 3.2 Package Orientation..... 8
 - 3.3 Pin Description..... 9
 - 3.4 Typical Application Circuits 10
 - 3.5 Tape and Reel 11
- 4 Specifications..... 13
 - 4.1 Absolute Maximum Ratings..... 13
 - 4.2 Sensor Characteristics 14
 - 4.3 Electrical and Timing Characteristics..... 15
 - 4.3.1 Electrical Power and Internal Characteristics..... 15
 - 4.3.2 I2C Electrical Characteristics 16
 - 4.3.3 I2C Timing Characteristics 17
- 5 General Operation 18
 - 5.1 Sensor Sampling..... 18
 - 5.2 Offset and Gain Calibration 18
 - 5.3 Tap Detection..... 18
- 6 Operational States 19
- 7 Operational State Flow 20
- 8 Interrupts..... 21
 - 8.1 Enabling and Clearing Interrupts 21
 - 8.2 ACQ_INT Interrupt 21
- 9 Sampling..... 22
 - 9.1 Continuous Sampling 22
- 10 I2C Interface 23
 - 10.1 Physical Interface..... 23
 - 10.2 Timing 24
 - 10.3 I2C Message Format..... 24
 - 10.4 Watchdog Timer..... 25

11	Register Interface	26
11.1	Register Summary	27
11.2	SR Status Register.....	30
11.3	OPSTAT Device Status Register.....	31
11.4	INTEN Interrupt Enable Register.....	32
11.5	MODE Register.....	33
11.6	SRTFR Sample Rate and Tap Feature Register	34
11.7	TAPEN Tap Control Register	35
11.8	TTTRX,TTTRY, TTTRZ X, Y and Z Tap Duration and Threshold Registers	36
11.9	XOUT_EX, YOUT_EX & ZOUT_EX X, Y, Z-Axis Acceleration Registers	37
11.10	OUTCFG Output Configuration Register	38
11.11	X-Axis Offset Registers	39
11.12	Y-Axis Offset Registers	40
11.13	Z-Axis Offset Registers	41
11.14	X-Axis Gain Registers	42
11.15	Y-Axis Gain Registers	43
11.16	Z-Axis Gain Registers	44
11.17	PCODE Product Code.....	45
12	Index of Tables	46
13	Revision History.....	47
14	Legal.....	48

1 ORDER INFORMATION

Table 1. Order Information

Part Number	Resolution	Order Number	Package	Shipping
MC3451	8 to 14-bit	MC3451	LGA-12	Tape & Reel, 5Ku

XXYM ● CCC	Row	Marking
	XXYM	Device identifier and date code
	CCC	Factory lot code
	●	Pin 1 identifier

Table 2. Package Information

2 FUNCTIONAL BLOCK DIAGRAM

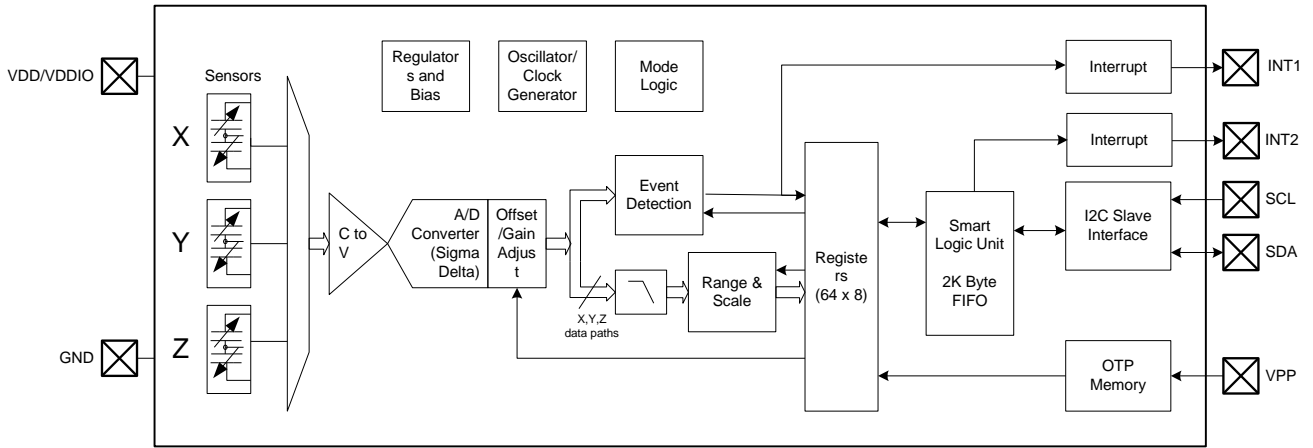


Figure 1. Block Diagram

3 PACKAGING AND PIN DESCRIPTION

3.1 PACKAGE OUTLINE

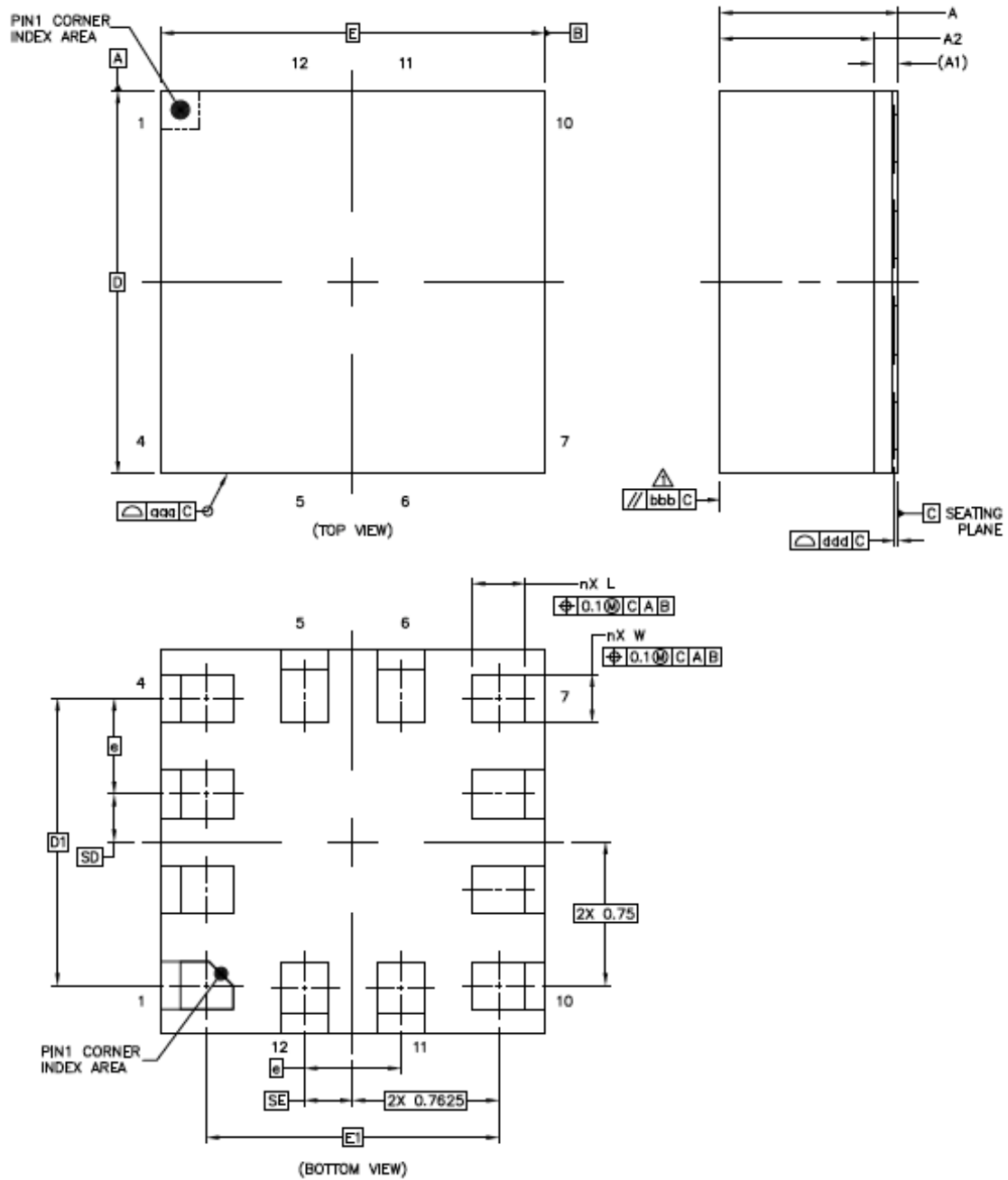


Figure 2. Package Outline and Mechanical Dimensions

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	0.86	0.93	1
SUBSTRATE THICKNESS	A1	0.13		REF
MOLD THICKNESS	A2	0.8		REF
BODY SIZE	D	2		BSC
	E	2		BSC
LEAD WIDTH	W	0.2	0.25	0.3
LEAD LENGTH	L	0.225	0.275	0.325
LEAD PITCH	e	0.5		BSC
LEAD COUNT	n	12		
EDGE BALL CENTER TO CENTER	D1	1.5		BSC
	E1	1.525		BSC
BODY CENTER TO CONTACT BALL	SD	0.25		BSC
	SE	0.25		BSC
BALL WIDTH	b	---	---	---
BALL DIAMETER		---		
BALL OPENING		---		
BALL PITCH	e1	---		
BALL COUNT	n1	---		
PRE-SOLDER		---	---	---
PACKAGE EDGE TOLERANCE	aaa	0.1		
MOLD FLATNESS	bbb	0.2		
COPLANARITY	ddd	0.08		
BALL OFFSET (PACKAGE)	eee	---		
BALL OFFSET (BALL)	fff	---		

Figure 3. Package Outline and Mechanical Dimensions

3.2 PACKAGE ORIENTATION

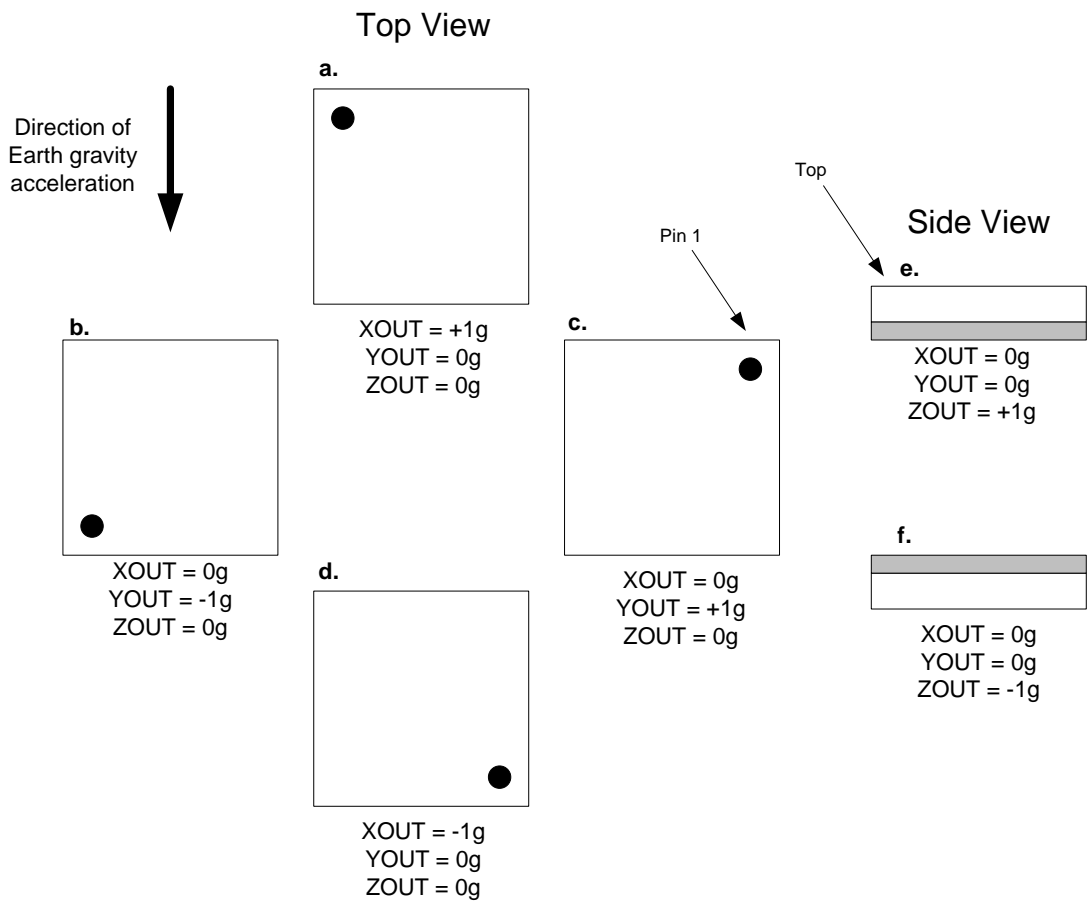


Figure 4. Package Orientation

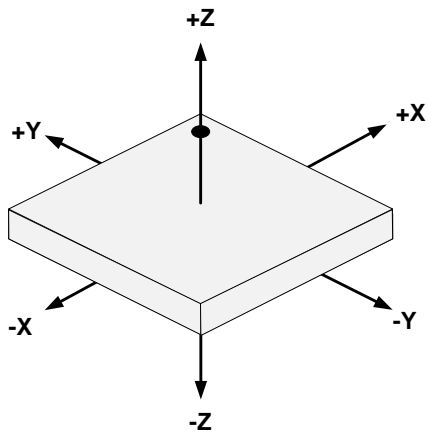


Figure 5. Package Axis Reference

3.3 PIN DESCRIPTION

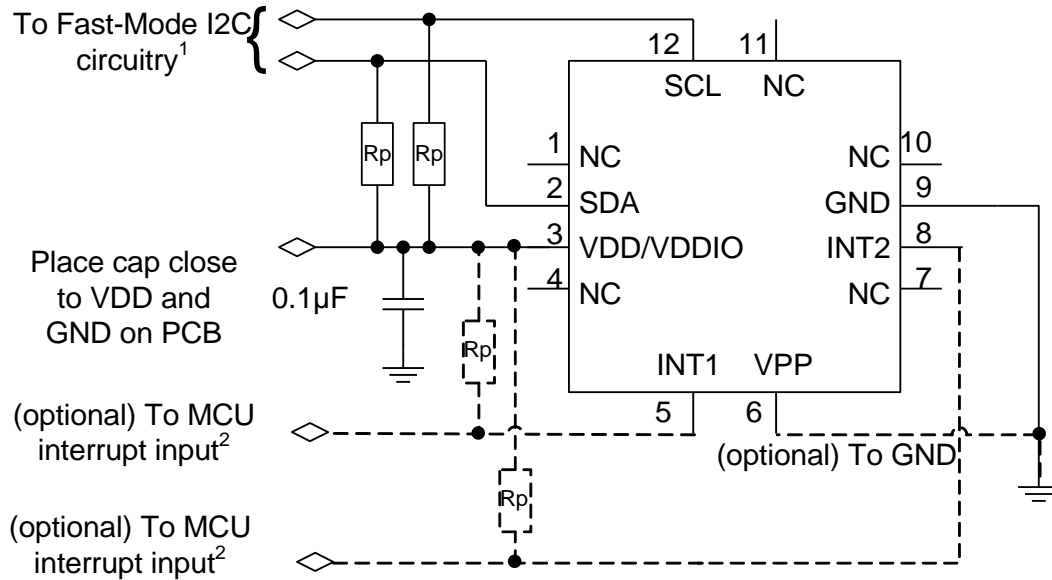
Pin	Name	Function
1	RES	No connect ¹
2	SDA ²	I2C serial data input/output
3	VDD/VDDIO	Power supply
4	RES	No connect
5	INT1 ³	Interrupt active LOW ⁴
6	VPP	Connect to GND/VDD/NC
7	NC	No connect
8	INT2	Interrupt active LOW ⁴
9	GND	Ground
10	RES	No connect
11	RES	No connect
12	SCL ²	I2C serial clock input

Table 3. Pin Description

Notes:

- 1) Pins which are labeled 'No Connect' are not internally connected to anything. They can be connected to any signal or be left floating.
- 2) These pins require a pull-up resistor, typically 4.7kΩ to pin VDD/VDDIO. Refer to I2C Specification for Fast-Mode devices. Higher resistance values can be used (typically done to reduce current leakage) but such applications are outside the scope of this datasheet.
- 3) This pin can be configured by software to operate either as an open-drain output or push-pull output (MODE Register). If set to open-drain, then it requires a pull-up resistor, typically 4.7kΩ to pin VDD/VDDIO.
- 4) INTN pin polarity is programmable in the MODE Register.

3.4 TYPICAL APPLICATION CIRCUITS



NOTE¹: Rp are typically 4.7k ohm pullup resistors to VDD/VDDIO, per I2C specification. When pin VDD/VDDIO is powered down, SDA and SCL will be driven low by internal ESD diodes.

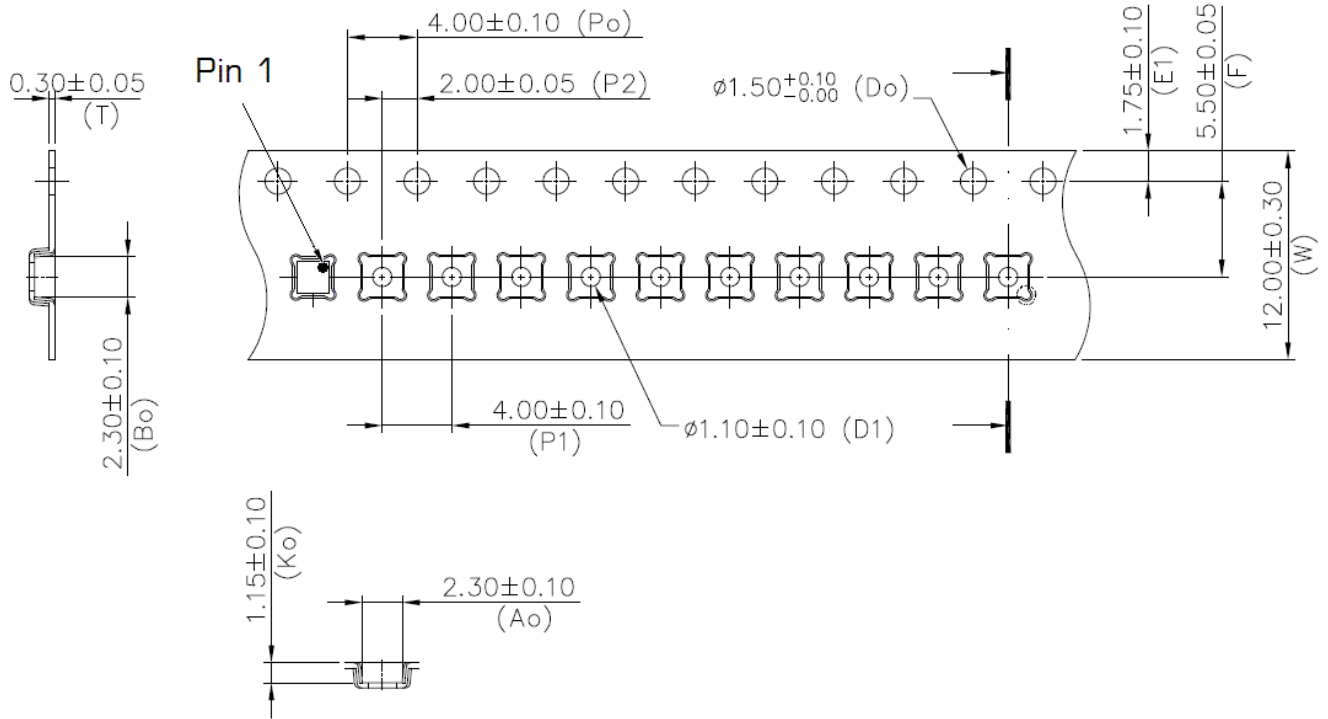
NOTE²: Attach typical 4.7k ohm pullup resistor if INTN is defined as open-drain.

Figure 6. Typical Application Circuit for 3DOF Solution

In typical applications, the interface power supply may contain significant noise from external sources and other circuits which should be kept away from the sensor. Therefore, for some applications a lower-noise power supply might be desirable to power the VDD/VDDIO pin.

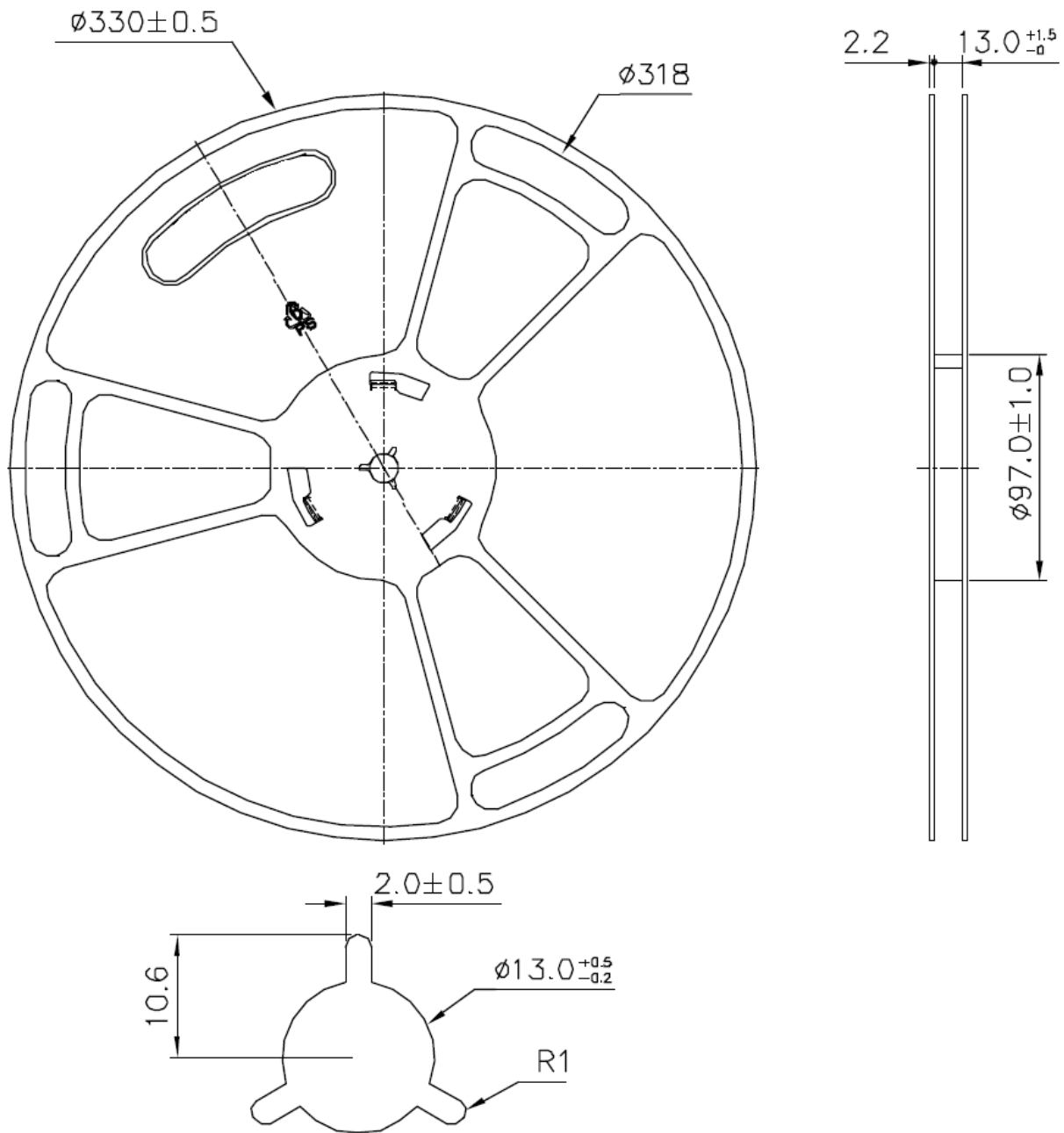
3.5 TAPE AND REEL

Devices are shipped in reels, in standard cardboard box packaging. See [Figure 4. MC3451 Tape Dimensions](#) and [Figure 5. MC3451 Reel Dimensions](#).



- Dimensions in mm.
- 10 sprocket hole pitch cumulative tolerance ± 0.2
- Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Figure 4. MC3451 Tape Dimensions



- Dimensions in mm.

Figure 5. MC3451 Reel Dimensions

4 SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS

Parameters exceeding the Absolute Maximum Ratings may permanently damage the device.

Rating	Symbol	Minimum / Maximum Value	Unit
Supply Voltages	Pin VDD/VDDIO	-0.3 / +3.6	V
Acceleration, any axis, 100 μ s	g_{MAX}	10000	g
Ambient operating temperature	T_{OP}	-40 / +85	$^{\circ}C$
Storage temperature	T_{STG}	-40 / +125	$^{\circ}C$
ESD human body model	HBM	± 2000	V
Latch-up current at $T_{op} = 25^{\circ}C$	I_{LU}	200	mA
Input voltage to non-power pin	Pins INTN, SCL and SDA	-0.3 / (VDD + 0.3) or 3.6 whichever is lower	V

Table 4. Absolute Maximum Ratings

4.2 SENSOR CHARACTERISTICS

VDD = 2.8V, T_{op} = 25 °C unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
Acceleration range	Resolution and range set in <u>OUTCFG Output Configuration Register</u>		±2 ±4 ±8 ±12 ±16		g
Sensitivity	Depends on settings in <u>OUTCFG Output Configuration Register</u>	8		4096	LSB/g
Sensitivity Temperature Coefficient ¹	-10 ≤ T _{op} ≤ +55 °C		± 0.025		%/°C
Zero-g Offset			± 20		mg
Zero-g Offset Temperature Coefficient ¹	-10 ≤ T _{op} ≤ +55 °C		± 1		mg/°C
Noise Density ¹			X,Y: 125 Z: 200		µg/√Hz
Nonlinearity ¹			2		% FS
Cross-axis Sensitivity ¹	Between any two axes		2		%

Table 5. Sensor Characteristics

¹ Values are based on device characterization, not tested in production.

4.3 ELECTRICAL AND TIMING CHARACTERISTICS

4.3.1 ELECTRICAL POWER AND INTERNAL CHARACTERISTICS

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Supply voltage ²	Pin VDD/VDDIO	VDD	1.7		3.6	V
Sample Rate Tolerance ³		Tclock	-10		10	%

Test condition: VDD = 2.8V, T_{op} = 25 °C unless otherwise noted

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Standby current		I _{ddsb}		5		µA
WAKE state supply current	Vdd = 1.8V, sample rate dependent	I _{dd}		1.3		mA
GESTURE state supply current	25Hz	I _{dd}		300		µA
Pad Leakage	Per I/O pad	I _{pad}	-1	0.01	1	µA

Table 6. Electrical Characteristics

² Min and Max limits are hard limits without additional tolerance.

³ Values are based on device characterization, not tested in production.

4.3.2 I2C ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
LOW level input voltage	VIL	-0.5	0.3*VDD	V
HIGH level input voltage	VIH	0.7*VDD	-	V
Hysteresis of Schmitt trigger inputs	Vhys	0.05*VDD	-	V
Output voltage, pin INTN, I _{ol} ≤ 2 mA	V _{ol}	0	0.4	V
	V _{oh}	0	0.9*VDD	V
Output voltage, pin SDA (open drain), I _{ol} ≤ 1 mA	V _{ols}	-	0.1*VDD	V
Input current, pins SDA and SCL (input voltage between 0.1*VDD and 0.9*VDD max)	I _i	-10	10	μA
Capacitance, pins SDA and SCL ⁴	C _i	-	10	pF

Table 7. I2C Electrical and Timing Characteristics

NOTES:

- If multiple slaves are connected to the I2C signals in addition to this device, only 1 pull-up resistor on each of SDA and SCL should exist. Also, care must be taken to not violate the I2C specification for capacitive loading.
- When pin VDD/VDDIO is not powered and set to 0V, INTN, SDA and SCL will be held to VDD plus the forward voltage of the internal static protection diodes, typically about 0.6V.
- When pin VDD/VDDIO is disconnected from power or ground (e.g. Hi-Z), the device may become inadvertently powered up through the ESD diodes present on other powered signals.

⁴ Values are based on device characterization, not tested in production.

4.3.3 I2C TIMING CHARACTERISTICS

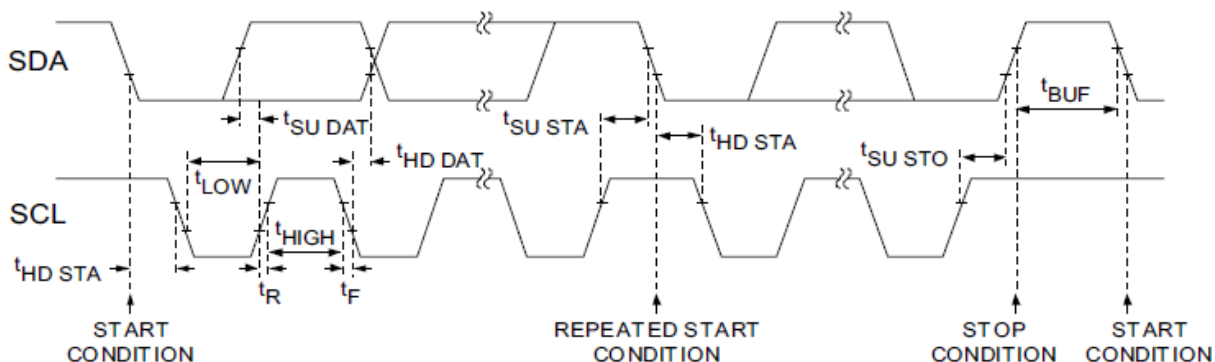


Figure 6. I2C Interface Timing

Parameter	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD,STA}$	Hold time (repeated) START condition	4.0	-	0.6	-	μ s
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	μ s
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	μ s
$t_{SU,STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	μ s
$t_{HD,DAT}$	Data hold time	5.0	-	-	-	μ s
$t_{SU,DAT}$	Data set-up time	250	-	100	-	ns
$t_{SU,STO}$	Set-up time for STOP condition	4.0	-	0.6	-	μ s
t_{BUF}	Bus free time between a STOP and START	4.7	-	1.3	-	μ s

Table 8. I2C Timing Characteristics

NOTE: Values are based on I2C Specification requirements, not tested in production.

See also Section [10.3 I2C Message Format](#).

5 GENERAL OPERATION

The device supports the reading of samples and device status upon interrupt or via polling.

5.1 SENSOR SAMPLING

Measurement data is stored in the “extended” registers XOUT_EX, YOUT_EX, and ZOUT_EX. The byte with the lower address of the byte pair is the least significant byte while the byte with the next higher address is the most significant byte. The measurement data is represented as 2’s complement format.

The desired resolution and full scale acceleration range are set in OUTCFG Output Configuration Register.

5.2 OFFSET AND GAIN CALIBRATION

Digital offset and gain calibration can be performed on the sensor, if necessary, in order to reduce the effects of post-assembly influences and stresses which may cause the sensor readings to be offset from their factory values.

5.3 TAP DETECTION

The device supports directional tap detection in $\pm X$, $\pm Y$ or $\pm Z$. Each axis is independent, although only one direction per axis is supported simultaneously. The threshold, duration, and dead-time of tap detection can be set for each axis, and six flag/status bits are maintained in a status register. The tap hardware uses a second order high-pass filter to detect fast impulse/transition acceleration events. The external interrupt pin can be used to indicate that a tap event has been detected.

5.4 PEDOMETER

The MC3451 has an integrated smart logic unit that can perform an internal algorithm for pedometer processing. This unit utilizes the 2K byte FIFO and outputs a 32-bit pedometer count. This configurable, high-accuracy algorithm is initialized after the device is powered on. It can meet a wide variety of pedometer requirements that are typically encountered in walking environments. For further details on this algorithm, please refer to the associated application note for the MC3451.

5.5 ANY MOTION AND GESTURE

The integrated smart logic unit also can perform “any motion” detection interrupt. This detection combined with motion continuance and tilt detection will allow the device to perform gesture recognition. For further details on this algorithm, please refer to the associated application note for the MC3451.

6 OPERATIONAL STATES

The device has four states of operation: INITIAL(default state), STANDBY, GESTURE and WAKE.

The device defaults to the INITIAL state waiting for initialization. Smart Logic Unit initial registers and Accelerometer registers allow Read/Write.

The STANDBY state offers the lowest power consumption. In this state, the I2C interface is inactive and all register reads and writes are disallowed. There is no event detection, sampling, or acceleration measurement in the STANDBY state. Internal clocking is halted. Complete access to the register set is allowed in this state, but interrupts cannot be serviced. The time to change states from STANDBY & GESTURE to WAKE is 200 μ s.

The GESTURE state offers the low power with Pedometer and Gesture recognize enable, the I2C interface be disabled except Smart Logic Unit been visit or INT2 I/O Wake.

The WAKE state enable full response to the I2C interface, including write access to all registers.

State	I2C Bus	Description
INITIAL	Device responds to I2C bus (R/W)	Device is powered; Registers can be accessed via I2C. No interrupt generation, Bypass enable. Default power-on state.
STANDBY	Device no responds to I2C Bus	Lowest power mode. Wake up from INT2 Voltage level change (High to Low/Low to high)
GESTURE	Device no responds to I2C Bus	Low power mode with Accelerometer and Smart Logic Unit power on
WAKE	Device responds to I2C bus (R/W)	Full running mode, sample rate up to 1024Hz, 2K bytes FIFO enable

Table 9. Operational States

7 OPERATIONAL STATE FLOW

Figure 7. shows the operational state flow for the device. The device defaults to INITIAL mode following power-on.

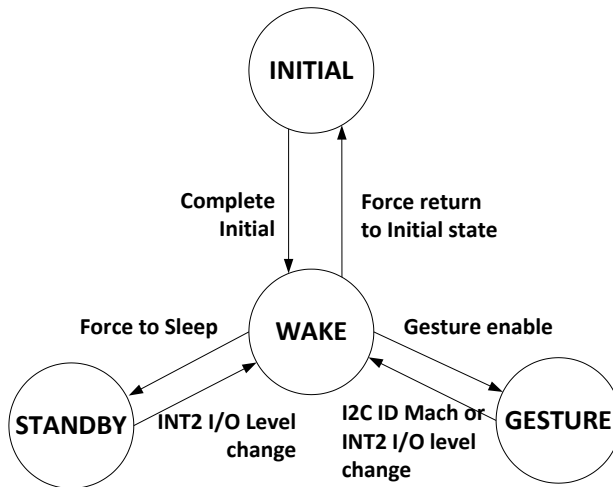


Figure 7. Operational State Flow

Action	Setting	Effect
Power on/ Force to INITIAL	CTL[7:0] = 0x5A	<ul style="list-style-type: none"> Switch to INITIAL state and stay there Waiting for initialize operation
Force WAKE State	CTL[7:0] = 0x55, 0xAA	<ul style="list-style-type: none"> Switch to WAKE state and stay there enable sensor and full functions
Force GESTURE State	MODE[7:0] = 0x01	<ul style="list-style-type: none"> Switch to GESTURE state and stay there Accelerometer and Smart Gesture unit in Low Power Mode
Force STANDBY State	MODE[7:0] = 0x02	<ul style="list-style-type: none"> All functions disabled

Table 10. Forcing Operational States

8 INTERRUPTS

The sensor device utilizes output pin INTN to signal to an external microprocessor that an event has been sensed. The microprocessor would contain an interrupt service routine which would perform certain tasks after receiving this interrupt and reading the associated status bits, perhaps after a sample was made ready. If interrupts are to be used, the microprocessor must set up the registers in the sensor so that when a specific event is detected, the microprocessor would receive the interrupt and the interrupt service routine would be executed. If polling is used there is no need for the interrupt registers to be set up.

For products that will instead use polling, the method of reading sensor data would be slightly different. Instead of receiving an interrupt when an event occurs, the microprocessor must periodically poll the sensor and read status data (the INTN pin is not used). For most applications, this is likely best done at the sensor sampling rate or faster.

Note that at least one I2C STOP condition must be present between samples in order for the sensor to update the sample data registers.

8.1 ENABLING AND CLEARING INTERRUPTS

The SR Status Register contains the flag bits for the sample acquisition interrupt ACQ_INT. The INTEN Interrupt Enable Register determines if a flag event generates interrupts.

The flags (and interrupts) are cleared and rearmed each time the SR Status Register is read. When an event is detected, it is masked with a flag bit in the INTEN Interrupt Enable Register, and then the corresponding status bit is set in the SR Status Register.

The polarity and driving mode of the external interrupt signal may be chosen by setting the IPP and IAH bits in the MODE Register.

8.2 ACQ_INT INTERRUPT

The ACQ_INT flag bit in the SR Status Register is always active. This bit is cleared when it is read. When a sample has been produced, an interrupt will be generated only if the ACQ_INT_EN bit in the INTEN Interrupt Enable Register is active. Note that the frequency of this ACQ_INT bit being set active is always the same as the sample rate.

9 SAMPLING

9.1 CONTINUOUS SAMPLING

The device has the ability to read all sampled readings in a continuous sampling fashion. The device always updates the XOUT, YOUT, and ZOUT registers at the chosen ODR.

An optional interrupt can be generated each time the sample registers have been updated (ACQ_INT interrupt bit in the INTEN Interrupt Enable Register). See Sections 8.2 and SR Status Register for ACQ_INT operation and options.

10 I2C INTERFACE

10.1 PHYSICAL INTERFACE

The I2C slave interface operates at a maximum speed of 400 kHz. The SDA (data) is an open-drain, bi-directional pin and the SCL (clock) is an input pin.

The device always operates as an I2C slave.

An I2C master initiates all communication and data transfers and generates the SCL clock that synchronizes the data transfer. The I2C device address depends upon the state of the VPP pin during power-up as shown in the table below.

An optional I2C watchdog timer reset can be enabled to prevent bus stall conditions. When enabled, the sensor I2C circuitry will reset itself if the master takes too long to issue clocks to the sensor during a read cycle (i.e. if there is a gap in SCL clocks of more than about 200mSec). A status bit can be read to observe if this condition has occurred.

<u>7-bit Device ID</u>	<u>8-bit Address</u> = Write	<u>8-bit Address</u> = Read	<u>VPP level</u> <u>upon</u> <u>power</u>	<u>Module</u>
0x4C (0b1001100)	0x98	0x99	GND	Accelerometer
0x6C (0b1101100)	0xD8	0xD9	VDD	Accelerometer
0x2D (0b0101010)	0x5A	0x5B	NA	Smart Gesture Unit

Table 11. I2C Address Selection

Internally, the registers which are used to store samples are clocked by the sample clock gated by I2C activity. Therefore, in order to allow the device to collect and present samples in the sample registers at least one I2C STOP condition must be present between samples.

Refer to the I2C specification for a detailed discussion of the protocol. Per I2C requirements, SDA is an open drain, bi-directional pin. SCL and SDA each require an external pull-up resistor, typically 4.7kΩ.

10.2 TIMING

See Section 4.3.3 I2C Timing Characteristics for I2C timing requirements.

10.3 I2C MESSAGE FORMAT

Note that at least one I2C STOP condition must be present between samples in order for the sensor to update the sample data registers.

The device uses the following general format for writing to the internal registers. The I2C master generates a START condition, and then supplies the 7-bit device ID. The 8th bit is the R/W# flag (write cycle = 0). The device pulls SDA low during the 9th clock cycle indicating a positive ACK.

The second byte is the 8-bit register address of the device to access, and the last byte is the data to write.

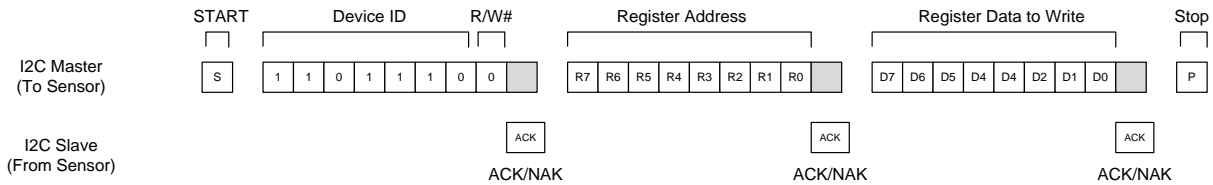


Figure 8. I2C Message Format, Write Cycle, Single Register Write

In a read cycle, the I2C master writes the device ID (R/W#=0) and register address to be read. The master issues a RESTART condition and then writes the device ID with the R/W# flag set to ‘1’. The device shifts out the contents of the register address.

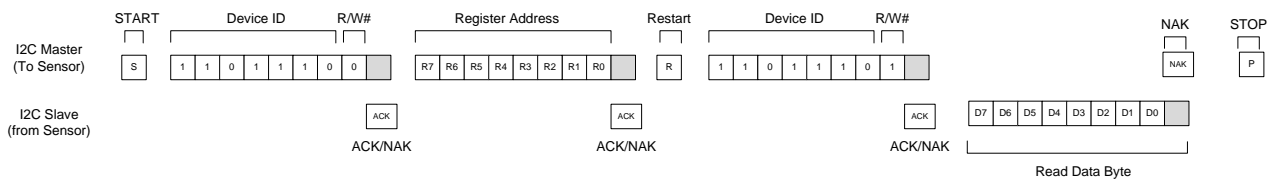


Figure 9. I2C Message Format, Read Cycle, Single Register Read

The I2C master may write or read consecutive register addresses by writing or reading additional bytes after the first access. The device will internally increment the register address.

If an I2C burst read operation reads past register address 0x12 the internal address pointer “wraps” to address 0x03 and the contents of the SR Status Register are returned.

10.4 WATCHDOG TIMER

When enabled (see [MODE Register](#)), the I2C watchdog timer prevents bus stall conditions in cases where the master does not provide enough clocks to the slave to complete a read cycle.

During a read cycle, the slave that is actively driving the bus (SDA pin) will not release the bus until 9 SCL clock edges are detected. While the SDA pin is held low by a slave open-drain output, any other I2C devices attached to the sample bus will be unable to communicate. If the slave does not see 9 SCL clocks from the master within the timeout period, the slave will assume a system problem has occurred and so the I2C circuitry will be reset, the SDA pin released and the sensor made ready for additional I2C commands.

No other changes to registers are made.

When enabled, the I2C watchdog timer does not resolve why the master did not provide enough clocks to complete a read cycle, but it does prevent a slave from holding the bus indefinitely.

When enabled, the timeout period is about 200mSec.

When an I2C watchdog timer event is triggered, the I2C_WDT bit in register will be set active by the Watchdog timer hardware. External software can detect this status by noticing this bit is active. The act of reading register 0x04 will clear the status.

11 REGISTER INTERFACE

The device has a simple register interface which allows a MCU or I2C master to configure and monitor all aspects of the device. This section lists an overview of user programmable registers. By convention, Bit 0 is the least significant bit (LSB) of a byte register.

11.1 REGISTER SUMMARY

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W ⁵
0x00-0x02	RESERVED ⁶											
0x03	SR	Status Register	ACQ_INT	Resv	TAP_ZN	TAP_ZP	TAP_YN	TAP_YP	TAP_XN	TAP_XP	0x00	R
0x04	OPSTAT	Operational Device Status Register	OTPA	Resv	Resv	I2C_WDT	Resv	Resv	OPSTAT [1]	OPSTAT [0]	0x00	R
0x05	RESERVED											
0x06	INTEN	Interrupt Enable Register	ACQ_INT_EN	Resv	TIZNEN	TIZPEN	TIYNEN	TIYPEN	TIXNEN	TIXPEN	0x00	W
0x07	MODE	Mode Register	IAH	IPP	I2C_WDT_POS	I2C_WDT_NEG	Resv	0 ⁷	OPCON [1]	OPCON [0]	0x00	W
0x08	SRTFR	Sample Rate and Tap Feature Register	TAP_LATCH	FLIP_TAPZ	FLIP_TAPY	FLIP_TAPX	RATE[3]	RATE[2]	RATE[2]	RATE[0]	0x00	W
0x09	TAPEN	Tap Control Register	TAP_EN	THRDUR	TAPZNEN	TAPZPEN	TAPYNEN	TAPYPEN	TAPXNEN	TAPXPEN	0x00	W
0x0A	TTTRX	X Tap Duration and Threshold Register	TTTRX[7]	TTTRX[6]	TTTRX[5]	TTTRX[4]	TTTRX[3]	TTTRX[2]	TTTRX[1]	TTTRX[0]	0x00	W
0x0B	TTTRY	Y Tap Duration and Threshold Register	TTTRY[7]	TTTRY[6]	TTTRY[5]	TTTRY[4]	TTTRY[3]	TTTRY[2]	TTTRY[1]	TTTRY[0]	0x00	W
0x0C	TTTRZ	Z Tap Duration and Threshold Register	TTTRZ[7]	TTTRZ[6]	TTTRZ[5]	TTTRZ[4]	TTTRZ[3]	TTTRZ[2]	TTTRZ[1]	TTTRZ[0]	0x00	W
0x0D	XOUT_EX_L	XOUT Extended Register	XOUT_EX[7]	XOUT_EX[6]	XOUT_EX[5]	XOUT_EX[4]	XOUT_EX[3]	XOUT_EX[2]	XOUT_EX[1]	XOUT_EX[0]	0x00	R
0x0E	XOUT_EX_H	XOUT Extended Register	XOUT_EX[15]	XOUT_EX[14]	XOUT_EX[13]	XOUT_EX[12]	XOUT_EX[11]	XOUT_EX[10]	XOUT_EX[9]	XOUT_EX[8]	0x00	R
0x0F	YOUT_EX_L	YOUT Extended Register	YOUT_EX[7]	YOUT_EX[6]	YOUT_EX[5]	YOUT_EX[4]	YOUT_EX[3]	YOUT_EX[2]	YOUT_EX[1]	YOUT_EX[0]	0x00	R
0x10	YOUT_EX_H	YOUT Extended Register	YOUT_EX[15]	YOUT_EX[14]	YOUT_EX[13]	YOUT_EX[12]	YOUT_EX[11]	YOUT_EX[10]	YOUT_EX[9]	YOUT_EX[8]	0x00	R
0x11	ZOUT_EX_L	ZOUT Extended Register	ZOUT_EX[7]	ZOUT_EX[6]	ZOUT_EX[5]	ZOUT_EX[4]	ZOUT_EX[3]	ZOUT_EX[2]	ZOUT_EX[1]	ZOUT_EX[0]	0x00	R
0x12	ZOUT_EX_H	ZOUT Extended Register	ZOUT_EX[15]	ZOUT_EX[14]	ZOUT_EX[13]	ZOUT_EX[12]	ZOUT_EX[11]	ZOUT_EX[10]	ZOUT_EX[9]	ZOUT_EX[8]	0x00	R
0x13-0x1F	RESERVED											
0x20	OUTCFG	Output Configuration Register	0 ⁷	RANGE[2]	RANGE[1]	RANGE[0]	Resv	RES[2]	RES[1]	RES[0]	0x00	W
0x21	XOFFL	X-Offset LSB Register	XOFF[7]	XOFF[6]	XOFF[5]	XOFF[4]	XOFF[3]	XOFF[2]	XOFF[1]	XOFF[0]	Per chip	W
0x22	XOFFH	X-Offset MSB Register	XGAIN[8]	XOFF[14]	XOFF[13]	XOFF[12]	XOFF[11]	XOFF[10]	XOFF[9]	XOFF[8]	Per chip	W
0x23	YOFFL	Y-Offset LSB Register	YOFF[7]	YOFF[6]	YOFF[5]	YOFF[4]	YOFF[3]	YOFF[2]	YOFF[1]	YOFF[0]	Per chip	W
0x24	YOFFH	Y-Offset MSB Register	YGAIN[8]	YOFF[14]	YOFF[13]	YOFF[12]	YOFF[11]	YOFF[10]	YOFF[9]	YOFF[8]	Per chip	W
0x25	ZOFFL	Z-Offset LSB Register	ZOFF[7]	ZOFF[6]	ZOFF[5]	ZOFF[4]	ZOFF[3]	ZOFF[2]	ZOFF[1]	ZOFF[0]	Per chip	W
0x26	ZOFFH	Z-Offset MSB Register	ZGAIN[8]	ZOFF[14]	ZOFF[13]	ZOFF[12]	ZOFF[11]	ZOFF[10]	ZOFF[9]	ZOFF[8]	Per chip	W
0x27	XGAIN	X Gain Register	XGAIN[7]	XGAIN[6]	XGAIN[5]	XGAIN[4]	XGAIN[3]	XGAIN[2]	XGAIN[1]	XGAIN[0]	Per chip	W

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W ⁵
0x28	YGAIN	Y Gain Register	YGAIN[7]	YGAIN[6]	YGAIN[5]	YGAIN[4]	YGAIN[3]	YGAIN[2]	YGAIN[1]	YGAIN[0]	Per chip	W
0x29	ZGAIN	Z Gain Register	ZGAIN[7]	ZGAIN[6]	ZGAIN[5]	ZGAIN[4]	ZGAIN[3]	ZGAIN[2]	ZGAIN[1]	ZGAIN[0]	Per chip	W
0x2A-0x3A	RESERVED											
0x3B	PCODE	Product Code Register	0	0	0	1	*8	*8	*8	0	Per chip	R
0x3C to 0x3F	RESERVED											

Table 12. Register Summary⁹

⁵ ‘R’ registers are read-only, via external I2C access. ‘W’ registers are read-write, via external I2C access.

⁶ Registers designated as ‘RESERVED’ should not be accessed by software.

⁷ Software must always write a zero ‘0’ to this bit.

⁸ Bits denoted with ‘*’ might be any value, set by the factory. Software should ignore these bits.

⁹ No registers are updated with new event status or samples while a I2C cycle is in process.

11.2 SR STATUS REGISTER

This register contains the flag/event bits for tap detection and sample acquisition. The TAP bits will only transition if the corresponding enable bit has been set in register 0x09, the TAP control register. Each read to this register will clear the latched event(s) and re-arm the flag for the next event.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x03	TAPR	Tap Status Register	ACQ_INT	Resv	TAP_ZN	TAP_ZP	TAP_YN	TAP_YP	TAP_XN	TAP_XP	0x00	R

TAP_XP	Positive X-axis TAP detected, flag is set in polling mode or interrupt mode.
TAP_XN	Negative X-axis TAP detected, flag is set in polling mode or interrupt mode.
TAP_YP	Positive Y-axis TAP detected, flag is set in polling mode or interrupt mode.
TAP_YN	Negative Y-axis TAP detected, flag is set in polling mode or interrupt mode.
TAP_ZP	Positive Z-axis TAP detected, flag is set in polling mode or interrupt mode.
TAP_ZN	Negative Z-axis TAP detected, flag is set in polling mode or interrupt mode.
ACQ_INT	Sample has been acquired, flag bit is set in polling mode or interrupt mode. This bit cannot be disabled and is always set by hardware when a sample is ready. The host must poll at the sample rate or faster to see this bit transition.

Table 13. SR Status Register

11.3 OPSTAT DEVICE STATUS REGISTER

The device status register reports various conditions of the sensor circuitry.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x04	OPSTAT	Operational Device Status Register	OTPA	Resv	Resv	I2C_WDT	Resv	Resv	OPSTAT [1]	OPSTAT [0]	0x00	R

OPSTAT[1:0]	Sampling State Register Status, Wait State Register Status 00: Device is in STANDBY state, no sampling 01: Device is in WAKE state, sampling at set sample rate 10: Reserved 11: Reserved
I2C_WDT	I2C watchdog timeout 0: No watchdog event detected 1: Watchdog event has been detected by hardware, I2C slave state machine reset to idle. This flag is cleared by reading this register.
OTPA	One-time Programming (OTP) activity status 0: Internal memory is idle and the device is ready for use 1: Internal memory is active and the device is not yet ready for use

Table 14. OPSTAT Device Status Register

11.4 INTEN INTERRUPT ENABLE REGISTER

The interrupt enable register allows the flag bits for specific TAP and sample events to also trigger a transition of the external INTN pin. This is the only effect these bits have as the flag bits will be set/cleared in the SR Status Register regardless of which interrupts are enabled in this register.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x06	INTEN	Interrupt Enable Register	ACQ_INT_EN	Resv	TIZNEN	TIZPEN	TIYNEN	TIYPEN	TIXNEN	TIXPEN	0x00	W

TIXPEN	Positive X-axis TAP interrupt enable 0: Disabled (default) 1: Enabled. The corresponding TAP enable bit in register 0x09 must be enabled. The INTN pad will transition.
TIXNEN	Negative X-axis TAP interrupt enable 0: Disabled (default) 1: Enabled. The corresponding TAP enable bit in register 0x09 must be enabled. The INTN pad will transition.
TIYPEN	Positive Y-axis TAP interrupt enable 0: Disabled (default) 1: Enabled. The corresponding TAP enable bit in register 0x09 must be enabled. The INTN pad will transition.
TIYNEN	Negative Y-axis TAP interrupt enable 0: Disabled (default) 1: Enabled. The corresponding TAP enable bit in register 0x09 must be enabled. The INTN pad will transition.
TIZPEN	Positive Z-axis TAP interrupt enable 0: Disabled (default) 1: Enabled. The corresponding TAP enable bit in register 0x09 must be enabled. The INTN pad will transition.
TIZNEN	Negative Z-axis TAP interrupt enable 0: Disabled (default) 1: Enabled. The corresponding TAP enable bit in register 0x09 must be enabled. The INTN pad will transition.
ACQ_INT_EN	Generate Interrupt 0: Disable automatic interrupt on INTN pad after each sample (default). 1: Enable automatic interrupt on INTN pad after each sample.

Table 15. INTEN Interrupt Enable Register Settings

11.5 MODE REGISTER

The MODE register controls the active operating state of the device. This register can be written from either operational state (STANDBY or WAKE).

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x07	MODE	Mode Register	IAH	IPP	I2C_WDT_POS	I2C_WDT_NEG	Resv	0*	OPCON [1]	OPCON [0]	0x00	W

NOTE*: Software must always write a zero '0' to Bit 2.

OPCON [1:0]	00: STANDBY state (default)	Set Device Operational State. WAKE or STANDBY
	01: WAKE state	
	10: Reserved	
	11: Reserved	
I2C_WDT_NEG	0: I2C watchdog timer for negative SCL stalls disabled (default) 1: I2C watchdog timer for negative SCL stalls enabled	WDT for negative SCL stalls
I2C_WDT_POS	0: I2C watchdog timer for positive SCL stalls disabled (default) 1: I2C watchdog timer for positive SCL stalls enabled	WDT for positive SCL stalls
IPP	0: Interrupt pin INTN is open drain (default) and requires an external pull-up to pin VDD/VDDIO.	Interrupt Push Pull
	1: Interrupt pin INTN is push-pull. No external pull-up resistor should be installed.	
IAH	0: Interrupt pin INTN is active low (default)	Interrupt Active High
	1: Interrupt pin INTN is active high	

Table 16. MODE Register Functionality

11.6 SRTFR SAMPLE RATE AND TAP FEATURE REGISTER

This register sets the sampling output data rate (ODR) for sensor. The upper 4 bit control functions related to tap hardware. The lower 4 bits control the rate, as shown in the table below.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x08	SRTFR	Sample Rate and Tap Feature Register	TAP_LATCH	FLIP_TAPZ	FLIP_TAPY	FLIP_TAPX	RATE[3]	RATE[2]	RATE[1]	RATE[0]	0x00	W

RATE[3:0]	0000: 32 Hz (default) 0001: 16 Hz 0010: 8 Hz 0011: 4 Hz 0100: 2 Hz 0101: 1 Hz 0110: 0.5 Hz 0111: 0.25 Hz 1000: 64 Hz 1001: 128 Hz 1010: 256 Hz 1011: Reserved 1100: Reserved 1101: Reserved 1110: Reserved 1111: Reserved
FLIP_TAPX	0: X positive and X negative tap are not switched (default) 1: X positive and X negative tap are switched
FLIP_TAPY	0: Y positive and Y negative tap are not switched (default) 1: Y positive and Y negative tap are switched
FLIP_TAPZ	0: Z positive and Z negative tap are not switched (default) 1: Z positive and Z negative tap are switched
TAP_LATCH	0: Multiple TAPs (of those which are enabled) are detected and latched (default) 1: First TAP detected (e.g. of those enabled) is latched, all others ignored until serviced by reading register 0x03.

Table 17. SRTFR Register Functionality

11.7 TAPEN TAP CONTROL REGISTER

This register allows the enabling and disabling of tap detection for axes and direction. Bit 7 disables tap detection completely. Bit 6, switches the feature controlled by registers 0xA, 0xB, and 0xC. When bit 6 is ‘0’, the tap duration and quiet parameters are accessed in 0xA to 0xC, and when ‘1’ the tap detection threshold is accessed.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x09	TAPEN	Tap Control Register	TAP_EN	THRDUR	TAPZPEN	TAPZPEN	TAPYNEN	TAPYPEN	TAPXNEN	TAPXPEN	0x00	W

TAPXPEN	0: Disable positive tap detection on X-axis (default) 1: Enable positive tap detection on X-axis
TAPXNEN	0: Disable negative tap detection on X-axis (default) 1: Enable negative tap detection on X-axis
TAPYPEN	0: Disable positive tap detection on Y-axis (default) 1: Enable positive tap detection on Y-axis
TAPYNEN	0: Disable negative tap detection on Y-axis (default) 1: Enable negative tap detection on Y-axis
TAPZPEN	0: Disable positive tap detection on Z-axis (default) 1: Enable positive tap detection on Z-axis
TAPZPEN	0: Disable negative tap detection on Z-axis (default) 1: Enable negative tap detection on Z-axis
THRDUR	0: Registers 0xA, 0xB, 0xC point to tap duration and quiet period (default) 1: Registers 0xA, 0xB, 0xC point to tap threshold settings. See description of TTTRX, TTTRY and TTTRZ.
TAP_EN	0: All tap detection is disabled, regardless of bits [5:0] (default) 1: Tap detection is enabled, individual enables control detection (bits 5-1)

Table 18. TAPEN Register Settings

11.8 TTTRX, TTTRY, TTTRZ X, Y AND Z TAP DURATION AND THRESHOLD REGISTERS

These 3 registers allow control of both the tap duration settings and tap threshold settings, depending upon the setting of the THRDUR bit (bit 6) in the TAPEN register (0x09).

When THRDUR=0, the register meaning is as follows:

Addr	Name	Description	TTTRX[7]	TTTRX[6]	TTTRX[5]	TTTRX[4]	TTTRX[3]	TTTRX[2]	TTTRX[1]	TTTRX[0]	POR Value	R/W
0x0A	Tap X Quiet-Duration	TAP X Duration Register	TAP_X_QUIET[3]	TAP_X_QUIET[2]	TAP_X_QUIET[1]	TAP_X_QUIET[0]	TAP_X_DUR[3]	TAP_X_DUR[2]	TAP_X_DUR[1]	TAP_X_DUR[0]	0x00	W
0x0B	Tap Y Quiet-Duration	TAP Y Duration Register	TAP_Y_QUIET[3]	TAP_Y_QUIET[2]	TAP_Y_QUIET[1]	TAP_Y_QUIET[0]	TAP_Y_DUR[3]	TAP_Y_DUR[2]	TAP_Y_DUR[1]	TAP_Y_DUR[0]	0x00	W
0x0C	Tap Z Quiet-Duration	TAP Z Duration Register	TAP_Z_QUIET[3]	TAP_Z_QUIET[2]	TAP_Z_QUIET[1]	TAP_Z_QUIET[0]	TAP_Z_DUR[3]	TAP_Z_DUR[2]	TAP_Z_DUR[1]	TAP_Z_DUR[0]	0x00	W

When THRDUR=1, the register meaning is as follows:

Addr	Name	Description	TTTRX[7]	TTTRX[6]	TTTRX[5]	TTTRX[4]	TTTRX[3]	TTTRX[2]	TTTRX[1]	TTTRX[0]	POR Value	R/W
0x0A	Tap X Thresh	TAP X Threshold Register	TAP_X_TH[7]	TAP_X_TH[6]	TAP_X_TH[5]	TAP_X_TH[4]	TAP_X_TH[3]	TAP_X_TH[2]	TAP_X_TH[1]	TAP_X_TH[0]	0x00	W
0x0B	Tap Y Thresh	TAP Y Threshold Register	TAP_Y_TH[7]	TAP_Y_TH[6]	TAP_Y_TH[5]	TAP_Y_TH[4]	TAP_Y_TH[3]	TAP_Y_TH[2]	TAP_Y_TH[1]	TAP_Y_TH[0]	0x00	W
0x0C	Tap Z Thresh	TAP Z Threshold Register	TAP_Z_TH[7]	TAP_Z_TH[6]	TAP_Z_TH[5]	TAP_Z_TH[4]	TAP_Z_TH[3]	TAP_Z_TH[2]	TAP_Z_TH[1]	TAP_Z_TH[0]	0x00	W

TAP_X_DUR[3:0] TAP_Y_DUR[3:0] TAP_Z_DUR[3:0]	This 4-bit value (0 to 15) sets the maximum number of samples an event must qualify as a tap before it is rejected. For example, if the value is 4, a fast acceleration event which exceeded the threshold for more than 4 consecutive samples would not trigger a tap event.
TAP_X_QUIET[3:0] TAP_Y_QUIET[3:0] TAP_Z_QUIET[3:0]	This 4-bit value (0 to 15) sets the number of samples to be ignored after successful tap detection. Detection is rearmed after the specific number of samples has passed.
TAP_X_TH[7:0] TAP_Y_TH[7:0] TAP_Z_TH[7:0]	This 8-bit unsigned value sets the minimum magnitude a snap event must reach before a tap is considered detected. Setting this parameter to a higher value will effectively reject all but the largest acceleration events as tap. Some experimentation in the final form-factor may be needed to find an appropriate setting for a particular product.

Table 19. TTTRX, TTTRY and TTTRZ Register Settings

11.9 XOUT_EX, YOUT_EX & ZOUT_EX X, Y, Z-AXIS ACCELERATION REGISTERS

The measurements from sensors for the 3-axes are available in these 3 registers. The most-significant bit of the value is the sign bit, and is sign extended to the higher bits. Note that all 3 axes are sampled and updated simultaneously. If an I2C burst read operation reads past register address 0x12 the internal address pointer “wraps” to address 0x03 and the contents of the SR Status Register are returned. This allows application software to burst read the contents of the six extended registers and relevant device state registers in a single I2C read cycle.

Once an I2C start bit has been recognized by the sensor, registers will not be updated until an I2C stop bit has occurred. Therefore, if software desires to read the low and high byte registers ‘atomically’, knowing that the values have not been changed, it should do so by issuing a start bit, reading one register, then reading the other register then issuing a stop bit. Note that all 6 registers may be read in one burst with the same effect.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x0D	XOUT_EX_L	XOUT Extended Register	XOUT_EX[7]	XOUT_EX[6]	XOUT_EX[5]	XOUT_EX[4]	XOUT_EX[3]	XOUT_EX[2]	XOUT_EX[1]	XOUT_EX[0]	0x00	R
0x0E	XOUT_EX_H	XOUT Extended Register	XOUT_EX[15]	XOUT_EX[14]	XOUT_EX[13]	XOUT_EX[12]	XOUT_EX[11]	XOUT_EX[10]	XOUT_EX[9]	XOUT_EX[8]	0x00	R
0x0F	YOUT_EX_L	YOUT Extended Register	YOUT_EX[7]	YOUT_EX[6]	YOUT_EX[5]	YOUT_EX[4]	YOUT_EX[3]	YOUT_EX[2]	YOUT_EX[1]	YOUT_EX[0]	0x00	R
0x10	YOUT_EX_H	YOUT Extended Register	YOUT_EX[15]	YOUT_EX[14]	YOUT_EX[13]	YOUT_EX[12]	YOUT_EX[11]	YOUT_EX[10]	YOUT_EX[9]	YOUT_EX[8]	0x00	R
0x11	ZOUT_EX_L	ZOUT Extended Register	ZOUT_EX[7]	ZOUT_EX[6]	ZOUT_EX[5]	ZOUT_EX[4]	ZOUT_EX[3]	ZOUT_EX[2]	ZOUT_EX[1]	ZOUT_EX[0]	0x00	R
0x12	ZOUT_EX_H	ZOUT Extended Register	ZOUT_EX[15]	ZOUT_EX[14]	ZOUT_EX[13]	ZOUT_EX[12]	ZOUT_EX[11]	ZOUT_EX[10]	ZOUT_EX[9]	ZOUT_EX[8]	0x00	R

Table 20. Extended Accelerometer Registers

11.10 OUTCFG OUTPUT CONFIGURATION REGISTER

This register can be used to set the range and resolution of the accelerometer measurements.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x20	OUTCFG	Output Configuration Register	0*	RANGE[2]	RANGE[1]	RANGE[0]	Resv	RES[2]	RES[1]	RES[0]	0x00	W

NOTE*: Software must always write a zero '0' to Bit 7.

RES[2:0]	<u>Accelerometer g Resolution</u> 000: Select 6-bits for accelerometer measurements (Default) 001: Select 7-bit for accelerometer measurements 010: Select 8-bit for accelerometer measurements 011: Select 10-bit for accelerometer measurements 100: Select 12-bit for accelerometer measurements 101: Select 14-bit for accelerometer measurements 110: Reserved 111: Reserved
RANGE[2:0]	<u>Accelerometer g Range</u> 000: Select +/- 2g range (Default) 001: Select +/- 4g range 010: Select +/- 8g range 011: Select +/- 16g range 100: Select +/- 12g range 101: Reserved 111: Reserved

Table 21. OUTCFG Resolution and Range Select Register Settings

11.11 X-AXIS OFFSET REGISTERS

This register contains a signed 2’s complement 15-bit value applied as an offset adjustment to the output of the sensor values, prior to being sent to the OUT_EX registers. The Power-On-Reset value for each chip is unique and is set as part of factory calibration. If necessary, this value can be overwritten by software.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x21	XOFFL	X-Offset LSB Register	XOFF[7]	XOFF[6]	XOFF[5]	XOFF[4]	XOFF[3]	XOFF[2]	XOFF[1]	XOFF[0]	Per chip	W
0x22	XOFFH	X-Offset MSB Register	XGAIN[8]	XOFF[14]	XOFF[13]	XOFF[12]	XOFF[11]	XOFF[10]	XOFF[9]	XOFF[8]	Per chip	W

11.12 Y-AXIS OFFSET REGISTERS

This register contains a signed 2’s complement 15-bit value applied as an offset adjustment to the output of the sensor values, prior to being sent to the OUT_EX registers. The Power-On-Reset value for each chip is unique and is set as part of factory calibration. If necessary, this value can be overwritten by software.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x23	YOFFL	Y-Offset LSB Register	YOFF[7]	YOFF[6]	YOFF[5]	YOFF[4]	YOFF[3]	YOFF[2]	YOFF[1]	YOFF[0]	Per chip	W
0x24	YOFFH	Y-Offset MSB Register	YGAIN[8]	YOFF[14]	YOFF[13]	YOFF[12]	YOFF[11]	YOFF[10]	YOFF[9]	YOFF[8]	Per chip	W

11.13 Z-AXIS OFFSET REGISTERS

This register contains a signed 2’s complement 15-bit value applied as an offset adjustment to the output of the sensor values, prior to being sent to the OUT_EX registers. The Power-On-Reset value for each chip is unique and is set as part of factory calibration. If necessary, this value can be overwritten by software.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x25	ZOFFL	Z-Offset LSB Register	ZOFF[7]	ZOFF[6]	ZOFF[5]	ZOFF[4]	ZOFF[3]	ZOFF[2]	ZOFF[1]	ZOFF[0]	Per chip	W
0x26	ZOFFH	Z-Offset MSB Register	ZGAIN[8]	ZOFF[14]	ZOFF[13]	ZOFF[12]	ZOFF[11]	ZOFF[10]	ZOFF[9]	ZOFF[8]	Per chip	W

11.14 X-AXIS GAIN REGISTERS

The gain value is an unsigned 9-bit number.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x22	XOFFH	X-Offset MSB Register	XGAIN[8]	XOFF[14]	XOFF[13]	XOFF[12]	XOFF[11]	XOFF[10]	XOFF[9]	XOFF[8]	Per chip	W
0x27	XGAIN	X Gain Register	XGAIN[7]	XGAIN[6]	XGAIN[5]	XGAIN[4]	XGAIN[3]	XGAIN[2]	XGAIN[1]	XGAIN[0]	Per chip	W

11.15 Y-AXIS GAIN REGISTERS

The gain value is an unsigned 9-bit number.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x24	YOFFH	Y-Offset MSB Register	YGAIN[8]	YOFF[14]	YOFF[13]	YOFF[12]	YOFF[11]	YOFF[10]	YOFF[9]	YOFF[8]	Per chip	W
0x28	YGAIN	Y Gain Register	YGAIN[7]	YGAIN[6]	YGAIN[5]	YGAIN[4]	YGAIN[3]	YGAIN[2]	YGAIN[1]	YGAIN[0]	Per chip	W

11.16 Z-AXIS GAIN REGISTERS

The gain value is an unsigned 9-bit number.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x26	ZOFFH	Z-Offset MSB Register	ZGAIN[8]	ZOFF[14]	ZOFF[13]	ZOFF[12]	ZOFF[11]	ZOFF[10]	ZOFF[9]	ZOFF[8]	Per chip	W
0x29	ZGAIN	Z Gain Register	ZGAIN[7]	ZGAIN[6]	ZGAIN[5]	ZGAIN[4]	ZGAIN[3]	ZGAIN[2]	ZGAIN[1]	ZGAIN[0]	Per chip	W

11.17 PCODE PRODUCT CODE

This register returns a value specific to the part number of this mCube device, noted below.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x3B	PCODE	Product Code Register	0	0	0	1	*	*	*	0	Per chip	R

Note: Bits denoted with '*' might be any value, set by the factory. Software should ignore these bits.

12 INDEX OF TABLES

Table 1. Order Information.....	4
Table 2. Pin Description.....	9
Table 3. Absolute Maximum Ratings.....	13
Table 4. Sensor Characteristics.....	14
Table 5. Electrical Characteristics.....	15
Table 6. I2C Electrical and Timing Characteristics.....	16
Table 7. I2C Timing Characteristics.....	17
Table 8. Operational States.....	Error! Bookmark not defined.
Table 9. Forcing Operational States.....	Error! Bookmark not defined.
Table 10. I2C Address Selection.....	23
Table 11. Register Summary.....	29
Table 12. SR Status Register.....	30
Table 13. OPSTAT Device Status Register.....	31
Table 14. INTEN Interrupt Enable Register Settings.....	32
Table 15. MODE Register Functionality.....	33
Table 16. SRTFR Register Functionality.....	34
Table 17. TAPEN Register Settings.....	35
Table 18. TTRX, TTRY and TTRZ Register Settings.....	36
Table 19. Extended Accelerometer Registers.....	37
Table 20. OUTCFG Resolution and Range Select Register Settings.....	38

13 REVISION HISTORY

Date	Revision	Description
Aug 2017	APS-048-0050v0.1	Initial release

14 LEGAL

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